| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/883,539 | JACKSON ET AL. | |
| | Examiner | Art Unit | |
| | Jason M. Perilla | 2638 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed May 13, 2005*.

2. ☒ The allowed claim(s) is/are *Claims 2-10, 12-16, and 22-26 renumbered respectively as claims 1-19*.

3. ☒ The drawings filed on *04 January 2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20050718*.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## EXAMINER'S AMENDMENT

1. Claims 2-10, 12-16, and 22-26 are pending in the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Craig Plastrik (41254) on July 18, 2005.

The application has been amended as follows wherein the following versions of claims 2-7, 12-14, 22 and 23 replace all prior versions in their entirety:

2. A modulator comprising:

an offset QPSK modulator, said offset QPSK modulator operative for receiving input data and generating a first output signal representing ~~the modulation~~ a frequency value of said input data to be imposed on a carrier signal to effect offset QPSK modulation ~~of said input signal~~ and a second output signal representing an amplitude of said input data;

a frequency modulator comprising a sigma-delta modulator, said frequency modulator operative for receiving said first output signal generated by said offset QPSK modulator, and generating a control signal representing ~~the~~ a desired frequency of said carrier signal such that said carrier signal represents said input ~~signal~~ data offset QPSK modulated;

a phase-lock loop circuit comprising a voltage controlled oscillator for generating said carrier signal and a programmable frequency divider, said programmable frequency divider receiving said control signal as an input signal, said programmable frequency divider operative for changing ~~the~~ a frequency of the carrier signal in accordance with said control signal, and

an amplifier having variable gain for receiving and amplifying said carrier signal output by said phase-lock loop circuit, said second output signal controlling ~~the~~ an amount of gain of said amplifier; and

wherein said offset QPSK modulator comprises:

a demultiplexer for receiving said input data and generating I and Q quadrature signals corresponding to said input data;

a delay circuit operative for receiving said Q quadrature signal from said demultiplexer and for delaying the Q quadrature signal relative to the I quadrature signal;

a digital waveform generator operative for receiving said I quadrature signal output by said demultiplexer and said delayed Q quadrature signal output by said delay circuit, and for generating said first output signal ~~a digital signal indicating the modulation to be imposed on said carrier signal~~.

3. A modulator according to claim 2, wherein said offset QPSK modulator further comprises:

a first finite impulse response filter coupled to the output of said demultiplexer, said first finite impulse response filter receiving the I quadrature signal; and

wherein said delay circuit comprises:

a second finite impulse response filter coupled to the demultiplexer, and receiving the Q quadrature signal.

4. A modulator according to claim 2, wherein said digital waveform generator comprises:

a first lookup table circuit operative for performing an arctangent function, said first lookup table circuit comprising a read-only-memory device, said first lookup table circuit generating a digital output signal indicating ~~the~~ a phase of a modulation signal to be imposed on said carrier signal; and

a differentiator coupled to said first lookup table circuit and operative for generating a digital output signal indicating ~~the~~ a frequency of said modulation signal to be imposed on said carrier signal.

5. A modulator according to claim 2, wherein said phase-lock loop circuit further comprises:

a reference divider operative for reducing ~~the~~ a frequency of a reference signal by a predetermined factor;

a phase detector coupled to said reference divider and said programmable frequency divider, said phase detector operative for generating an error signal indicating ~~the~~ a frequency difference between a signal output by said reference divider and a signal output by said programmable frequency divider; and

a filter coupled to the output of said phase detector.

6. The modulator according to claim 2, wherein said control signal is programmable so as to allow said voltage controlled oscillator to be controlled to a the desired carrier frequency.

7. The modulator according to claim 2, further comprising a second lookup table for receiving said I quadrature signal and said delayed Q quadrature signal as input signals, and generating the second output signal indicating an amplitude of said ~~received~~ I quadrature signal and said delayed Q quadrature signal.

12. A modulator utilizing direct digital offset QPSK modulation, said ~~synthesizer~~ modulator comprising:

a digital offset QPSK modulator, said digital offset QPSK modulator operative for receiving ~~a~~ digital input data and generating a first digital output signal, said first digital output signal representing ~~the modulation~~ a frequency value of said digital input data to be imposed on a carrier signal to effect offset QPSK modulation ~~of said digital input signal~~ and a second digital output signal representing an amplitude of said digital input data;

a frequency modulator comprising a sigma-delta modulator, said frequency modulator operative for receiving said first digital output signal generated by said digital offset QPSK modulator, and generating a digital control signal representing ~~the~~ a desired frequency of said carrier signal such that said carrier signal represents said digital input ~~signal~~ data offset QPSK modulated;

a phase-lock loop circuit comprising a voltage controlled oscillator for generating said carrier signal and a programmable frequency divider, said programmable frequency divider receiving said digital control signal as an input signal, said programmable frequency divider operative for changing ~~the~~ a frequency of the carrier signal in accordance with said control signal; and

an amplifier having a variable gain for receiving and amplifying said carrier signal output by said phase-lock loop circuit, said second digital output signal controlling ~~the~~ an amount of gain of said amplifier; and

wherein said digital offset QPSK modulator comprises:

a digital demultiplexer for receiving said digital input data and generating I and Q quadrature signals corresponding to said digital input data;

a digital delay circuit operative for receiving said Q quadrature signal from said digital demultiplexer and for delaying the Q quadrature signal relative to the I quadrature signal; and

a digital waveform generator operative for receiving said I quadrature signal output by said digital demultiplexer and said delayed Q quadrature signal output by said digital delay circuit, and for generating said first digital output signal ~~a digital signal indicating the modulation to be imposed on said carrier signal~~.

13. A modulator according to claim 12, wherein said digital waveform generator comprises:

a first lookup table circuit operative for performing an arctangent function, said first lookup table circuit comprising a read-only-memory device, said first lookup table circuit generating a digital output signal indicating ~~the~~ a phase of a modulation signal to be imposed on said carrier signal; and

a digital differentiator coupled to said first lookup table circuit and operative for generating a digital output signal indicating ~~the~~ a frequency of said modulation signal to be imposed on said carrier signal.

14. The modulator according to claim 12, further comprising a second lookup table for receiving said I quadrature signal and said delayed Q quadrature signal as input signals, and generating the second output signal indicating an amplitude of said ~~received~~ I quadrature signal and said delayed Q quadrature signal.

22. A method for generating an offset QPSK modulated signal at a desired carrier frequency, said method comprising the steps of:

receiving an input data signal to be modulated;

generating a digital output signal representing ~~the modulation~~ a frequency value of said input data signal to be imposed on ~~said~~ a carrier signal to effect offset QPSK modulation of said input data signal;

generating an amplitude signal indicative of the amplitude of said input data signal;

utilizing a frequency modulator comprising a sigma-delta modulator to receive said digital output signal and to generate a digital control signal representing the desired frequency of said carrier signal such that said carrier signal represents said input ~~signal~~ data offset QPSK modulated;

controlling a programmable frequency divider forming a portion of a phase-lock loop circuit, said programmable frequency divider receiving said digital control signal as an input signal, said programmable frequency divider operative for changing ~~the~~ a frequency of said carrier signal in accordance with said digital control signal, said carrier signal being generated by a voltage controlled oscillator;

amplifying said carrier signal in accordance with ~~the~~ a level of said amplitude signal; and

wherein the step of generating a digital output signal representing a frequency value of said input data comprises:

demultiplexing said input data signal and generating digital I and Q quadrature signals corresponding to said input data signal;

delaying the Q quadrature signal relative to the I quadrature signal;

performing an arctangent function on said delayed Q quadrature signal and said I quadrature signal so as to generate an output signal indicating the phase of a modulation signal to be imposed on said carrier signal; and

differentiating said output signal so as to generate the digital output signal ~~a digital signal indicating the frequency of said modulation signal to be imposed on said carrier signal~~.

23. A method for generating an offset QPSK modulated signal at a desired carrier frequency according to claim 22, wherein said digital control signal is programmable so as to allow said voltage controlled oscillator to be controlled to ~~a~~ the desired carrier frequency.

Claims 2-10, 12-16, and 22-26 are renumbered respectively as claims 1-19, and the claim dependency is renumbered accordingly.

## *Allowable Subject Matter*

3. Claims 2-10, 12-16, and 22-26 are renumbered respectively as claims 1-19 are allowed.

4. The following is an examiner's statement of reasons for allowance:

Claims 2-10, 12-16, and 22-26 are renumbered respectively as claims 1-19 are allowed because the prior art of record does not disclose or obviate the claimed polar modulator having a frequency modulator comprising a sigma-delta modulator taking as input the output of an offset QPSK modulator comprising a demultiplexer, a delay circuit, and a digital waveform generator.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
July 18, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER